# DS1220Y
# 16K Nonvolatile SRAM

## FEATURES

.10 years minimum data retention in the absence of external power

.Data is automatically protected during power loss

.Directly replaces 2k x 8 volatile static RAM of EEPROM

.Unlimited write cycles

.Low-power CMOS

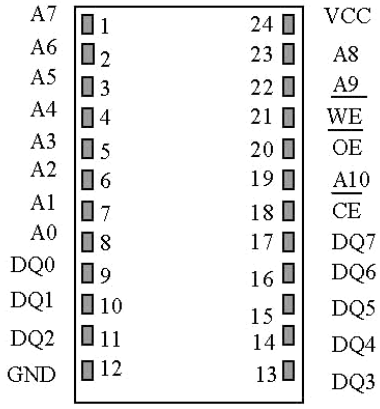
.JEDEC standard 24-pin DIP package

.Read and write access times as fast as 100ns

.Full ±10% operating range

.Optional industrial temperature range of -40℃ to +85℃, designated IND

**PIN ASSIGNMENT**




**24-Pin ENCAPSULATED PACKAGE**

**720-mil EXTENDED**

**PIN DESCRIPTION**

| | |
|---|---|
| A0-A10 | -Address Inputs |
| DQ0-DQ7 | -Data In/Data Out |
| $\overline{CS}$ | -Chip Enable |
| $\overline{WE}$ | -Write Enable |
| $\overline{OE}$ | -Output Enable |
| Vcc | -Power (+5V) |
| GND | -Ground |

**DESCRIPTION**

The DS1220Y 16K Nonvolatile SRAM is a 16, 384-bit, fully static, nonvolatile RAM organized as 2048 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors Vcc for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. The NV SRAM can be used in place of existing 2K x 8 SRAMs directly conforming to the popular bytewide 24-pin DIP standard. The DS1220Y also matches the pinout of the 2716 EPROM or the 2816 EEPROM, allowing direst substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing.

**READ MODE**

The DS1220Y executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 11 address inputs (A0-A10) defines which of the 2048 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within $t_{ACC}$ (Access Time) after the last address input signal is stable, providing the $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{CE}$ and OE access times are not satisfied, then data access must be measured from the later-occurring signal and the limiting parameter is either $t_{CO}$ for $\overline{CE}$ or $t_{OE}$ for $\overline{OE}$ rather than address access.

**WRITE MODE**

The DS1220Y executes a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are active (low) after address inputs are stable. The later-occurring falling earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time ($t_{WR}$) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in $t_{ODW}$ from its falling edge.

**DATA RETENTION MODE**

The DS1220Y provides full-functional capability for Vcc greater than 4.5 volts and write protects at 4.25 nominal. Data is maintained in the absence of Vcc without any additional support circuitry. The DS1220Y constantly monitors Vcc. Should the supply voltage decay, the NV SRAM automatically write protects itself, all inputs become "don't care," and all outputs become high-impedance. As Vcc falls below approximately 3.0 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when Vcc rises above approximately 3.0 volts, the power switching circuit connects external Vcc to RAM and disconnects the lithium energy source. Normal RAM operation can resume after Vcc exceeds 4.5 volts.

## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Voltage on Any Pin Relative to Ground | -0.3V to +7.0V |
| Operating Temperature | 0°C to 70°C; -40°C to +85°C for IND parts |
| Storage Temperature | -40°C to +70°C; -40°C to +85°C for IND parts |
| Soldering Temperature | 260°C for 10 seconds |

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS (TA: See Note 10)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Power Supply Voltage | Vcc | 4.5 | 5.0 | 5.5 | V | |
| Input Logic 1 | $V_{IH}$ | 2.2 | | Vcc | V | |
| Input Logic 0 | $V_{IL}$ | 0.0 | | +0.8 | V | |

## DC ELECTRICAL CHARACTERISTICS ($T_A$:See Note 10; Vcc=5V ±10%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{IL}$ | -1.0 | | +10 | µA | |
| I/O Leakage Current $\overline{CE} \geq V_{IH} \leq Vcc$ | $I_{IO}$ | -10 | | +1.0 | µA | |
| Output Current @ 2.4 V | $I_{OH}$ | -1.0 | | | mA | |
| Output Current @ 0.4V | $I_{OL}$ | 2.0 | | | mA | |
| Standby Current $\overline{CE}$=2.2V | $I_{CCSI}$ | | 3.0 | 7.0 | mA | |
| Standby Current $\overline{CE}$=Vcc-0.5V | $I_{CCS2}$ | | 2.0 | 4.0 | mA | |
| Operating Current $t_{CYC}$ =200ns (Commercial) | Icco1 | | | 75 | mA | |
| Operating Current $t_{CYC}$=200ns (Industrial) | Icco1 | | | 85 | mA | |
| Write Protection Voltage | $V_{TP}$ | | 4.25 | | V | |

## CAPACITANCE ($T_A$=25°C)

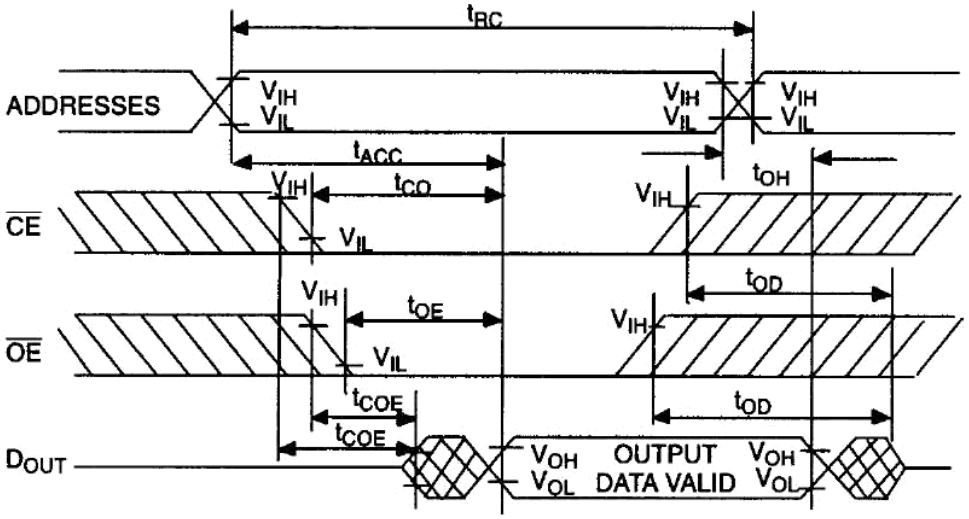
| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | | 5 | 10 | pF | |
| Input/Output Capacitance | $C_{I/O}$ | | 5 | 12 | pF | |

## AC ELECTRICAL CHARACTERISTICS

($T_A$: See Note 10; Vcc =5.0V ±10%)

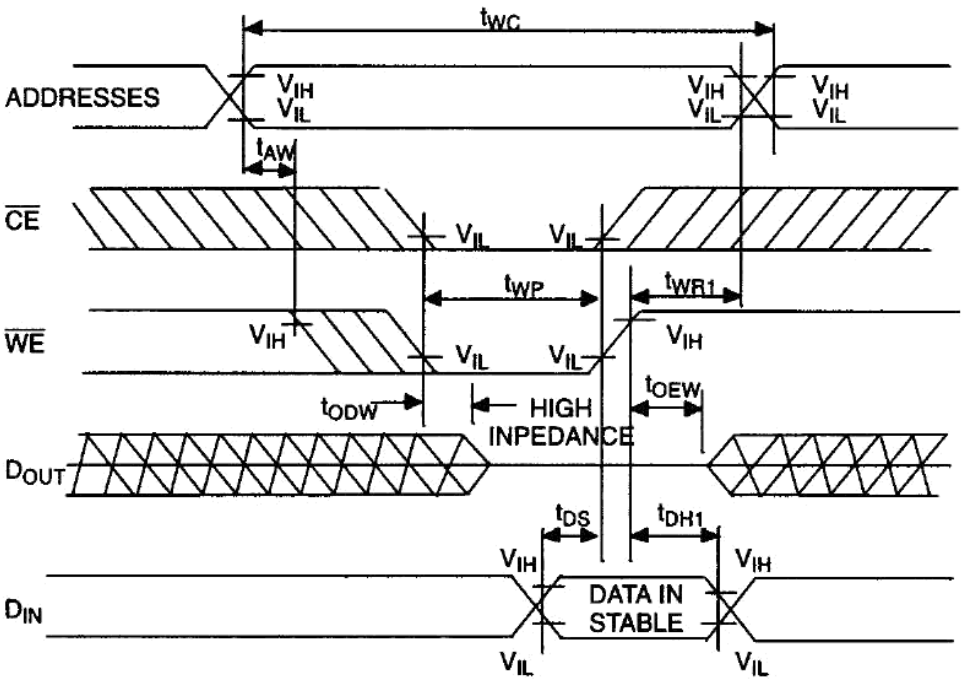
| PARAMETER | SYM | DS1220Y-100 | | DS1220Y-120 | | DS1220Y-150 | | DS1220Y-200 | | UNITS | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | |
| Read Cycle Time | $t_{RC}$ | 100 | | 120 | | 150 | | 200 | | ns | |
| Access Time | $t_{ACC}$ | | 100 | | 120 | | 150 | | 200 | ns | |
| $\overline{OE}$ to Output Valid | $t_{OE}$ | | 50 | | 60 | | 70 | | 100 | ns | |
| $\overline{OE}$ to Output Valid | $t_{CO}$ | | 100 | | 120 | | 150 | | 200 | ns | |
| $\overline{OE}$ or $\overline{CE}$ to Output Active | $t_{COE}$ | 5 | | 5 | | 5 | | 5 | | ns | 5 |
| Output High Z From Deslection | $t_{OD}$ | | 35 | | 35 | | 35 | | 35 | ns | 5 |
| Output Hold from Address Change | $t_{OH}$ | 5 | | 5 | | 5 | | 5 | | ns | |
| Write Cycle Time | $t_{WC}$ | 100 | | 120 | | 150 | | 200 | | ns | |
| Write Pulse Width | $t_{WP}$ | 75 | | 90 | | 100 | | 150 | | ns | 3 |
| Address SetupTime | $t_{AW}$ | 0 | | 0 | | 0 | | 0 | | ns | |
| Write Recovery Time | $t_{WR1}$<br>$t_{WR2}$ | 0<br>10 | | 0<br>10 | | 0<br>10 | | 0<br>10 | | ns<br>ns | 12<br>13 |
| Output High Z from $\overline{WE}$ | $t_{ODW}$ | | 35 | | 35 | | 35 | | 35 | ns | 5 |
| Output Active from $\overline{WE}$ | $t_{OEW}$ | 5 | | 5 | | 5 | | 5 | | ns | 4 |
| Data Setup Time | $t_{DS}$ | 40 | | 50 | | 60 | | 80 | | ns | 4 |
| Data Hold Time | $t_{DH1}$<br>$t_{DH2}$ | 0<br>10 | | 0<br>10 | | 0<br>10 | | 0<br>10 | | ns<br>ns | 12<br>13 |

## READ CYCLE



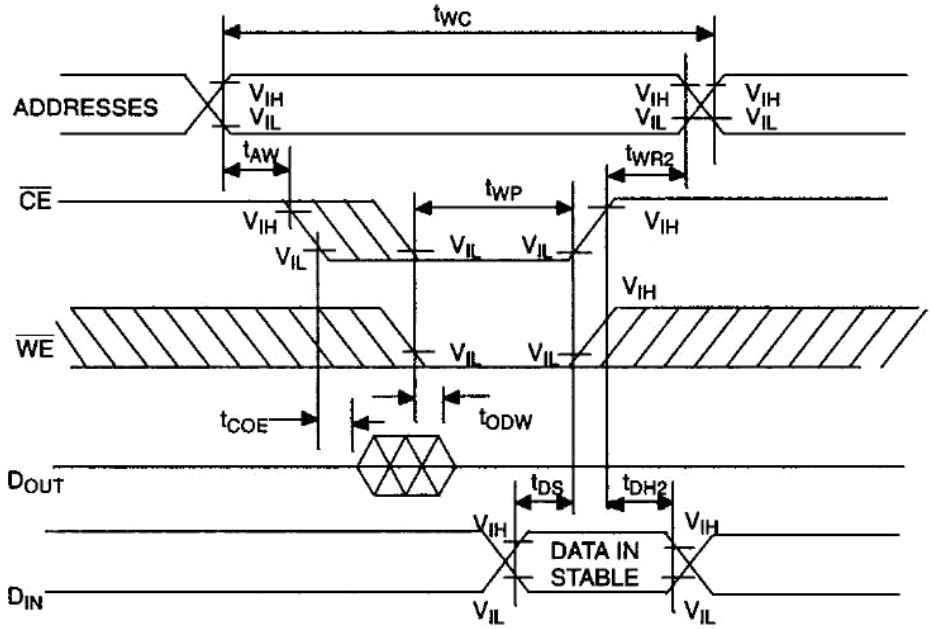

SEE NOTE1

**WRITE CYCLE 1**



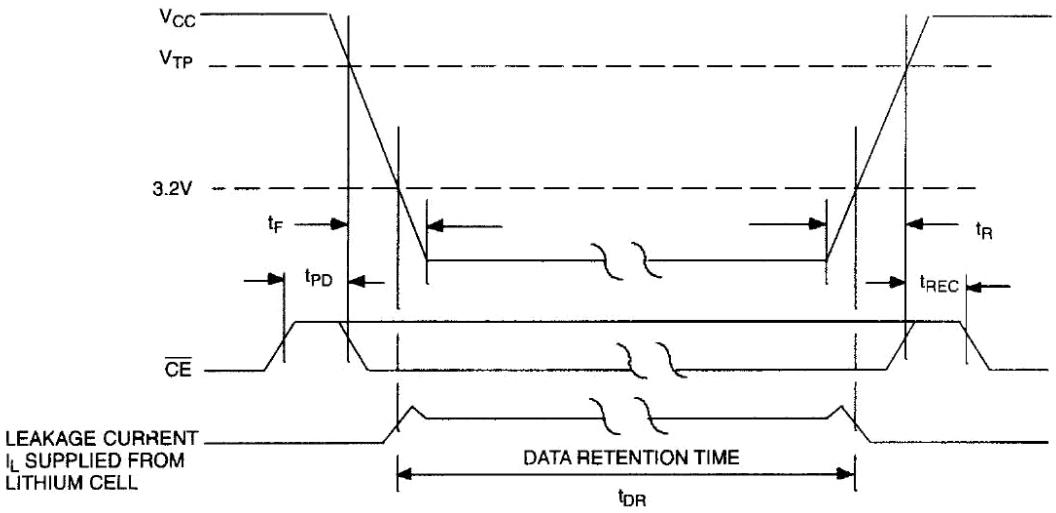

SEE NOTES 2,3,4,6,7,8 AND 12

**WRITE CYCLE 2**




SEE NOTE 2,3,4,6,7,8 AND 13

## POWER-DOWN/POWER-UP CONDITION




SEE NOTE 11

## POWER-DOWN/POWER-UP TIMING

| PARAMETER | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $\overline{CE}$ at $V_{IH}$ before Power-Down | $t_{PD}$ | 0 | | µs | 11 |
| $V_{CC}$ Slew from VTP to 0V | $t_F$ | 100 | | µs | |
| Vcc Slew from 0V to $V_{TP}$ | $t_R$ | 0 | | µs | |
| $\overline{CE}$ at $V_{IH}$ after Power -Up | $t_{REC}$ | | 2 | ms | |

($T_A$=25°C)

| PARAMETER | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Expected Data Retention Time | $t_{DR}$ | 10 | | years | 9 |

**WARNING:**

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

**NOTES:**

1.$\overline{WE}$ is high for a read cycle.

2.$\overline{OE}$ = $V_{IH}$ or $V_{IL}$. If $\overline{OE}$ = $V_{IH}$ during a write cycle, the output buffers remain in a high impedance state.

3.$t_{WP}$ is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. $t_{WP}$ is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.

4.$t_{DS}$ are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.

5.These parameters are sampled with a 5 pF load and are not 100% tested.

6.If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in write cycle 1, the output buffers remain in a high impedance state during this period.

7.If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.

8.If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.

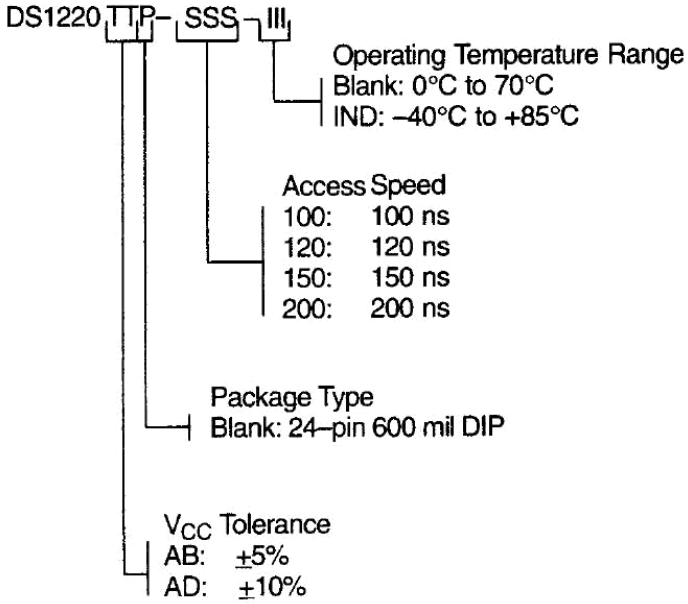
9.Each DS1220Y is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected $t_{DR}$ is defined as starting at the date of manufacture.

10.All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0 °C to 70°C. For industrial products (IND), this range is -40°C to +85°C.
11. In a power-down condition the voltage on any pin may not exceed the voltage of Vcc.
12.$t_{WR1}$, $t_{DH1}$ are measured from $\overline{WE}$ going high.
13.$t_{WR2}$,$t_{DH2}$ are measured from $\overline{CE}$ going high.
14.DS1220Y modules are recognized by Underwriters Laboratory (U.L ®) under file E99151 (R).

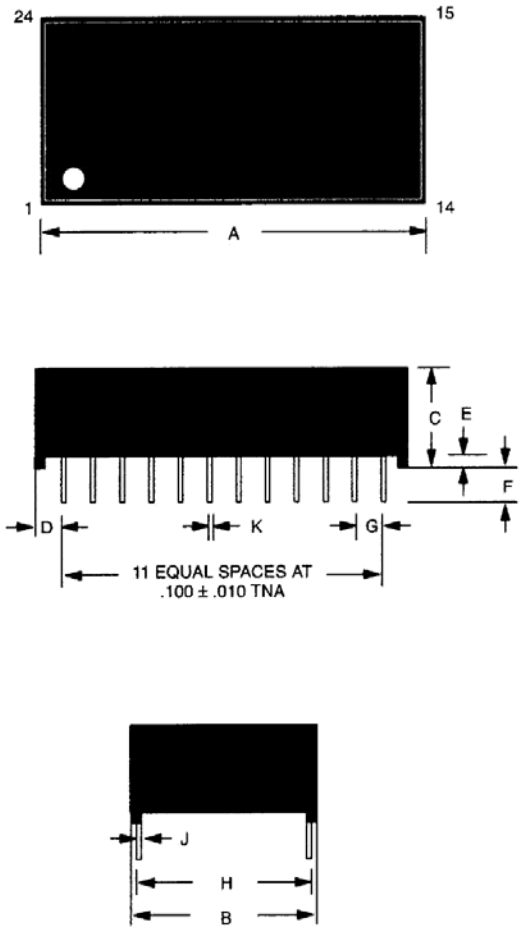
**DC TEST CONDITIONS**
Outputs open.
All voltages are referenced to ground.

**AC TEST CONDITIONS**
Output Load: 100pF +1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output 1.5V
Input Pulse Rise and Fall Times: 5ns

## ORDERING INFORMATION



## DS1220Y NONVOLATILE SRAM,24-PIN 720-MIL EXTENDED MODULE




| PKG | 24-PIN | |
|---|---|---|
| DIM | MIN | MAX |
| A IN. | 1.320 | 1.340 |
| MM | 33.53 | 34.04 |
| B IN. | 0.695 | 0.720 |
| MM | 17.65 | 18.29 |
| C IN. | 0.390 | 0.415 |
| MM | 9.91 | 10.54 |
| D IN. | 0.100 | 0.130 |
| MM | 2.54 | 3.30 |
| E IN. | 0.017 | 0.030 |
| MM | 0.43 | 0.76 |
| F IN. | 0.120 | 0.160 |
| MM | 3.05 | 4.06 |
| G IN. | 0.090 | 0.110 |
| MM | 2.29 | 2.79 |
| H IN | 0.590 | 0.630 |
| MM | 14.99 | 16.00 |
| J IN. | 0.008 | 0.012 |
| MM | 0.20 | 0.30 |
| K IN. | 0.015 | 0.021 |
| MM | 0.38 | 0.53 |